JSNM

Standard of Japan Society of Newer Metals

JSNM-SI-003A

Test method for determining resistivity of silicon epitaxial layer by usingevaporated metal Schottky diode capacitance-voltage measurements

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Prepared by

Epitaxial Layer Resistivity Evaluation WG

（Epitaxial Layer Resistivity Evaluation Standard Committee, concurrently）

Material Standards Study Group for Semiconductor Supply-Chain(M4S)

(Silicon Subcommittee Standardization Promotion Committee, concurrently）

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This document is a translation of JSNM standard in Japanese.
In the event of any doubt arising, the original standard in Japanese is to be evidenced.

Standard of Japan Society of Newer Metals

Test method for determining resistivity of silicon epitaxial layer by using evaporated metal Schottky diode capacitance-voltage measurements

1 Background

The resistivity of silicon epitaxial layers is a critical parameter in semiconductor device design. Controlling the resistivity of the epitaxial layer in the semiconductor device manufacturing process is crucial in determining the device's performance through the margin of the semiconductor device design. To enhance resistivity controllability, measuring the resistivity of a dummy epitaxial layer and providing feedback to the subsequent epitaxial growth condition are necessary. In the case of wafers containing the epitaxial layers, resistivity is an important inspection parameter required during the acceptance or incoming inspection of the wafer products.

Currently, test method for semiconductor resistivity using mercury as a Schottky electrode metal is available in the SEMI standard. However, determining the area of mercury contact is challenging, and there is a trend to restrict the use of mercury in the manufacturing process due to the Minamata Convention on Mercury (September 2019). Therefore, standardizing a non-mercury resistivity measurement method is desirable.

2 Scope

2.1 This standard provides the test method for resistivity by reverse bias voltage dependence of the capacitance of a Schottky junction diode (hereinafter referred to as C-V method), prepared on epitaxial layers, uniformly doped in depth- direction, grown on mirror-polished silicon substrates.

2.2 This standard is applicable for measuring the resistivity range of 0.08 Ω·cm ~ 110 Ω·cm for n-type silicon and 0.5 Ω·cm ~ 120 Ω·cm for p-type silicon.

2.3 The test method defined in this document is applicable for process control, material study, quality assurance, and material certification.

3 Referenced standard documents

The standards listed below are considered a part of this standard when referenced in this document.

3.1 SEMI standards

a) **SEMI MF42** : Test Method for Conductivity Type of Extrinsic Semiconducting Materials

b) **SEMI MF43** : Test Method for Resistivity of Semiconductor Materials

c) **SEMI MF723-0307E** : Practice for Conversion Between Resistivity and Dopant or Carrier Density for Boron-Doped, Phosphorous-Doped, and Arsenic-Doped Silicon

d) **SEMI MF1392** : Standard Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements with a Mercury Probe

e) **SEMI MF1527-1018**: Guide for Application of Certified Reference Materials and Reference Wafers for Calibration and Control of Instruments for Measuring Resistivity of Silicon

3.2 ISO Standards

a) **ISO14644-1** : Cleanrooms and Associated controlled environments Part1:Classification of Air cleanliness by particle concentration

3.3 Japan industrial standards (JIS)

a) JIS H 0602-1995 : Testing method of resistivity for silicon crystals and silicon wafers with four-point probe

4 Limitations

4.1 Limitation due to Destructive inspection

This method is a destructive inspection. Therefore, when this standard is adopted for trading epitaxial wafers, it will serve as quality assurance for the epitaxial wafers grown by the equipment conditioned using the resistivity measurement of the preceding epitaxial growth. The procedure for this preceding test growth and the product fabrication is determined by mutual agreement between the supplier and the customer.

4.2 Limitations due to the measurement principles

4.2.1 This measurement is based on the one-dimensional depletion layer approximation of semiconductor Schottky junctions and calculates the space charge density from the capacitance proportional to the Schottky electrode area. The capacitance attributed to the area around the electrode edge contributes to the errors. Therefore, the shape and size of the Schottky electrode should ensure that the capacitance proportional to the electrode area is substantially larger than the capacitance proportional to the length of the electrode edge. However, when the electrode area is made too large, there is a possibility that defects on the epitaxial layer will be picked up by the Schottky electrode, resulting in the deterioration of the Schottky characteristics.

4.2.2 The thickness of the epitaxial layer shall be greater than the thickness of the depletion layer formed at zero-bias condition of the Schottky barrier, and the front of the depletion layer shall not reach the interface between the epitaxial layer and the substrate when biased.

5 Measurement Principle

In this standard, the resistivity is measured using C-V method using Schottky junction. The system diagram is shown in Fig.1. The following relations are obtained among the reverse bias voltage V applied to the Schottky electrode, Schottky junction capacitance C, and carrier density $n(d)$ where d is the depth from the junction interface.

$$n(d) = \frac{2}{q\varepsilon_0\varepsilon_S A^2} \cdot \frac{dV}{d(C^{-2})} \quad \cdots\cdots \quad (1)$$

$$d = \frac{\varepsilon_0\varepsilon_S A}{C} \quad \cdots\cdots\cdots \quad (2)$$

where,

A : area of the electrode

q : electronic charge

ε_0 : electric permeability of vacuum

ε_S : relative electric permeability of silicon

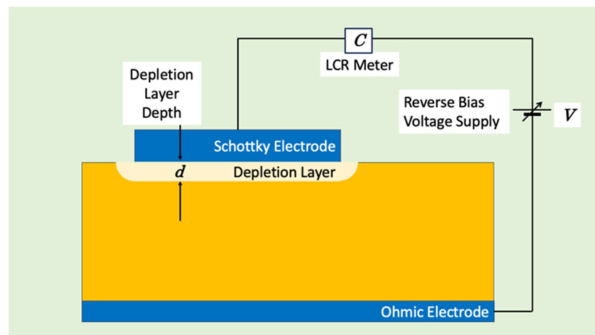

Fig.1 System diagram for *C-V* method

From these relations, carrier density depth profile is calculated using V and C as parameters.

6 Samples

6.1 Sampling Location

The measurement sample with Schottky diodes is made from target epitaxial wafers or chips obtained from the target wafer. It is recommended to fabricate multiple Schottky diodes are fabricated on a sample so that alternative diodes can be measured in case measured diode exhibit abnormal characteristics or is broken. The location of the Schottky diodes shall be selected that the resistivity measured by the Schottky diode will represent the wafer resistivity and determined by mutual agreement by the supplier and the customer, considering the characteristics of the epitaxial layer growth apparatus.

6.2 Sample Structure

There are two options for the sample structure regarding the position of the pseudo ohmic contacts of the Schottky diodes. One option is from the sample's back side (i.e. substrate), and the other is from the surface (i.e. epitaxial layer).

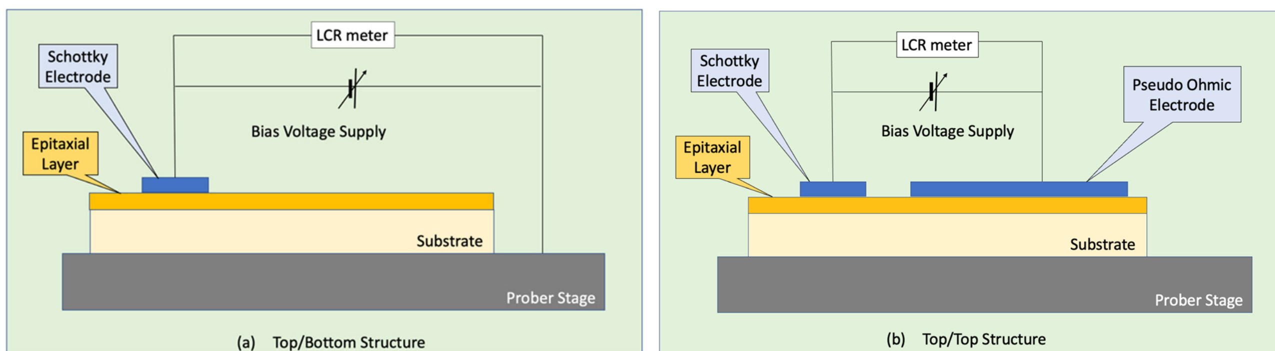

Fig.2 Sample Structures

a) Top / Bottom Structure

The sample structure, in which the Schottky junction is on the epitaxial layer, and the ohmic junction is on the sample back side. (Fig.2(a))

A Schottky electrode is fabricated on the epitaxial layer, and the mechanical contact between the sample's back surface and the metal prober stage is considered as a pseudo ohmic contact. The substrate shall be the same conduction type (n/p) as the epitaxial layer and shall not have non-conducting layer as oxide on the back-surface. The mechanical contact between the stage and the sample has large area and is forward biased during the measurements, so it can be considered as a pseudo-ohmic contact.

b) Top / Top Structure

The sample structure consists of both the Schottky junction and ohmic junctions are on the epitaxial layer (Fig.2(b)).
This configuration is necessary when the epitaxial layers are grown on high resistivity substrate or when the epitaxial layer and the substrate have different conduction types. The ohmic contact on the epitaxial layer is a large area Schottky electrode compared to the Schottky junction to be measured, and considered a pseudo ohmic contact.

6.3 Sample treatment before metal deposition

The characteristics of the Schottky diodes can deteriorate when the electrodes are placed on silicon crystal defects or if foreign material such as dirt, oxide etc. exist between the electrodes and the epitaxial layers. In such cases, the C-V curve deviates from the ideal case, leading to incorrect resistivity calculations. Therefore it is crucial that the Schottky diode is well fabricated for accurate measurements. To reduce the presence of foreign materials at the interface, the metal evaporation process shall be performed shortly after the completion of epitaxial growth. It is recommended that the air exposure period of the epitaxial wafer between growth and metal evaporation is less than three hours. Prolonged air exposure or storage in cases lead to surface contamination or natural oxides formation on the surface. In these situations, chemical treatments to remove contamination, foreign material, and oxides etc. from the epitaxial wafer surfaces shall be carried out just before electrode metal vacuum evaporation.
It is recommended that the surface treatment be performed in a cleanroom with a cleanliness class of 5 or less (according to ISO 14644-1).

6.4 Fabrication of Schottky Electrode

Schottky electrodes are formed by vacuum evaporation of Schottky metal on silicon wafers using stencil masks. Commonly used Schottky metals include gold for n-type silicon and antimony or aluminum for p-type silicon epitaxial layers. Schottky metal shall be of high purity; for gold, a purity of 3N or higher, and for aluminum, a purity of 5N or higher.
The size of the Schottky electrode is determined by the aperture of the stencil mask. For round apertures, a diameter of 2 mm ~ 4 mm is recommended.
During the fabrication of electrodes using a stencil mask, it is necessary to ensure that the evaporated electrode's shape and size does not deviate from those of the stencil mask, and not affected by shading attributed to the edge of the stencil masks. To achieve this, the following countermeasures can be considered;

a) Ensure that the flux of the evaporated metal perpendicular to the stencil mask.

b) Avoid mask deformation by metal deposition through mask maintenance.
c) Use a thinner stencil mask.
d) Make the evaporation source smaller.
e) Increase the thickness of the evaporation layer.

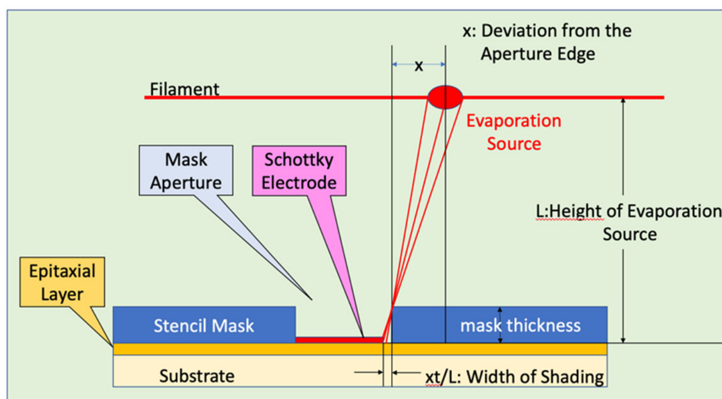

Fig. 3 Shading by a Stencil Mask

Epitaxial wafers or chips are loaded in the vacuum evaporation system, and after evacuation, deposition is performed. A vacuum below 10^{-3} Pa is recommended. The thickness of the Schottky electrodes shall be sufficient to avoid the punctuating by the contact of the prober needle. After the Schottky electrode evaporation, heat treatment of the sample shall be avoided to prevent metal impurity diffusion from the electrode or silicidation with the electrode.

7 Measurement

The manual procedure of data acquisition, analysis of C-V measurements is described below. If the data acquisition and analysis is performed using automatic measuring device, it shall be confirmed with the device and software manufacturer that the device operation procedure aligns with the procedure described in this section.

7.1Measurement Environment

The following measurement environment is recommended.

a) Temperature: 24 ℃ ± 3 ℃、 Relative Humidity: 30 % ～ 80 %
b) Illumination on the sample stage: Shaded or less than 500 lx

7.2 Device Calibration

Device calibration shall be performed before measurement according to the manufacture's manuals. This procedure is allowed to be skipped if the reproducibility of the data obtained by the device is guaranteed by regular calibration or an equivalent method.

7.3 C-V Measurement Condition

a) Find the rough guide for the conductivity type and resistivity of the substrate and epitaxial layer from the growth hysteresis. Based on the estimated resistivity of the sample, determine the range of reverse bias voltage for the C-V measurement. For this **Fig.1** of **SEMI MF1392** can be referred.
b) The overlapping alternative voltage frequency for capacitance measurements shall be 800 kHz ～1.0 MHz.

7.4 Measurement Circuit

Measurement shall be performed using the four-terminal method or an equivalent method to prevent the

voltage drop of the cables, etc. from affecting the data. The way the measurement system is grounded significantly affects the obtained data quality, so it is recommended to refer to the operating manual to ensure the stable ground connection. Special attention is necessary when the sample has an top/bottom structure, as the sample stage of the prober is likely grounded.

7.5 Procedure for C-V measurement

a) Connect the LCR meter to the prober and adjust it according to the manufacturer's manual. Also, collect the data on floating capacitance etc., required for analysis. If the measurement system configuration has not been changed, previous values can be used.

b) Place the sample on the sample stage of the prober and connect the prober needles to the Schottky and ohmic electrodes.

c) Measure the reverse bias voltage (V) dependence of the capacitance (C) while changing the reverse bias voltage in steps (δV). Record the measured values as pairs (C_i, V_i) of capacitance and voltage, where the subscript i indicates the i-th measurement value. Note that when the reverse bias voltage exceeds the reverse breakdown voltage of the Schottky junction, the leakage current increases, and the Schottky junction becomes unstable due to heating, eventually leading to destruction. In such cases, replace the Schottky device to be measured with a spare and perform the measurement again.

d) At least five pairs (C_i, V_i) of capacitance and voltage around the required depth shall be measured. However, when the breakdown voltage is low, it is allowed to use fewer measurement points.

e) After the measurement is complete, return the applied voltage to 0 V and remove the probe needles from the electrodes. Then, remove the sample from the sample stage.

7.6 Measurement of the electrode area of the sample

Measure the area A of the Schottky electrode on the measurement sample.

7.7 Calculation of carrier density and resistivity

a) Determine the depth-dependent carrier density $n(d)$ based on equations (1) and (2).

b) Since the measurement is in the room temperature range where the extrinsic semiconductor is in its saturation region, the calculated carrier density $n(d)$ is equal to the value at 23 °C regardless of the measurement temperature. Convert this value to the resistivity ρ at 23 °C using SEMI MF723 (defined at 23 °C).

8 Report

The content of the report data is determined by mutual agreement between the supplier and the customer. However, it is recommended to include the following items:

a) Date of measurement:

b) Measurement sample number:

c) Specification of the measured sample: growth specifications(substrate, impurity, resistivity,

thickness)

d) Structure of the measurement sample: "Top / Top" structure or "Top / Bottom" structure

e) Structure of the Schottky electrode: material, shape, thickness, area(specification, measured value)

f) Structure of the pseudo ohmic electrode: shape, designed area

g) Schottky characteristics: complex impedance (at zero-bias condition), I-V characteristics, etc.

h) Measurement data:

1) Maximum reverse bias voltage
2) Reverse bias step (incremental) voltage
3) i-th data, I = 1 to N (N is the number of measurements)

i) Overlapping AC for capacitance measurement: voltage, frequency

j) Measurement atmosphere: temperature, humidity, illumination

k) Measurement results: carrier density, resistivity, depth

l) Procedure for preparing the provided crystal: batch number after preparing the evaluation sample, etc.

m) Others: Deviation from the procedure described in this standard

9 Accuracy and Reliability

9.1 Simultaneous distribution-type interlaboratory tests was performed, and the variation in obtained resistivities according to this standard is shown blow. This variation is described in terms of the relative standard deviation (RSD: here, RSD = (standard deviation of each range) / (mean value of each range) × 100) calculated from the results measured in the range of 0.08 Ω·cm to 110 Ω·cm for n-type and 0.5 Ω·cm to 120 Ω·cm for p-type epitaxial layer.
The standard deviation used here is based on the population variance: the sum of squares of the deviation from the mean values of each institution divided by the number of institutions. The number of participated institutions is 4 for n-type and 3 for p-type.

9.1.1 The results of the interlaboratory test and the RSD among measurement institutions for n-type samples are shown in Figure 4 and Table 1. The RSD was 1.0% to 3.6% for the resistivity range of 0.08 Ω·cm to 110 Ω·cm , which is good.

9.1.2 Similarly, the results of the interlaboratory test and the RSD among measurement institutions for p-type samples are shown in Figure 5 and Table 2. The RSD was 1.8% to 3.2% in the range of 0.5 Ω·cm to 120 Ω·cm, which is also good.

9.3 From these results, it is indicated that when following this standard, the inter-institutional variation (RSD) for both n-type and p-type is operable at 5% or less.

Table 1. RSDs for Individual Instituion (n-type)

Nominal Resistivity (Ω·cm)	0.08	0.2	0.3	0.5	1	5	10	20	50	110
Institution A	0.0840	0.175	0.268	0.554	1.13	5.54	11.0	21.4	55.5	113
Institution B	0.0860	0.172	0.263	0.551	1.10	5.33	10.7	20.3	53.0	108
Institution C	0.0833	0.175	0.262	0.543	1.11	5.28	10.5	19.9	51.1	102
Institution D	0.0826	0.171	0.257	0.538	1.10	5.34	10.6	-	52.9	107
Average	0.0840	0.173	0.263	0.547	1.11	5.37	10.7	20.5	53.1	108
Standard Deviation	0.00126	0.00172	0.00393	0.00625	0.0133	0.0974	0.220	0.631	1.58	3.90
RSD(%)	**1.5%**	**1.0%**	**1.5%**	**1.1%**	**1.2%**	**1.8%**	**2.1%**	**3.1%**	**3.0%**	**3.6%**

Note: The absence of the data for institution D at 20Ω·cm is due to the limitation number of the samples in the interlaboratory test.

Table 2. RSDs for Individual Instituion (p-type)

Nominal Resistivity (Ω·cm)	0.5	1	5	10	20	50	120
Institution A	0.570	1.03	5.18	10.4	20.6	52.8	129
Institution B	0.527	0.974	4.87	9.79	19.7	49.8	121
Institution C	0.550	1.01	4.98	10.1	20.0	50.8	121
Average	0.549	1.00	5.01	10.1	20.1	51.1	123
Standard Deviation	0.0176	0.0235	0.128	0.256	0.363	1.24	3.84
RSD(%)	**3.2%**	**2.3%**	**2.6%**	**2.5%**	**1.8%**	**2.4%**	**3.1%**

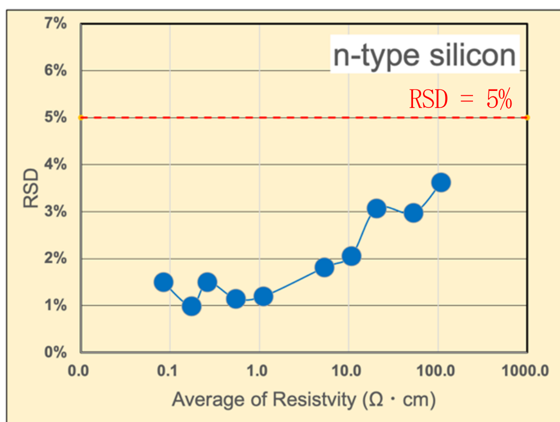

Fig. 4. RSD vs. Resistivity (n-type)

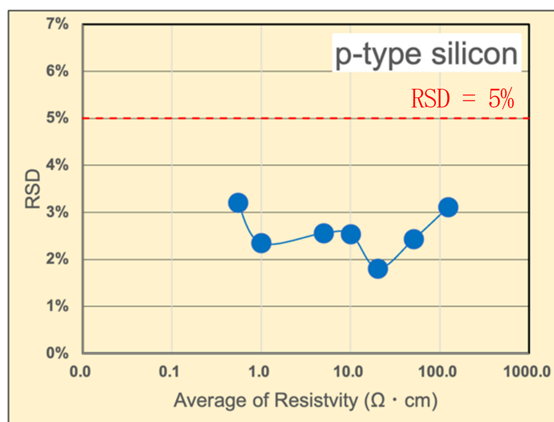

Fig. 5. RSD vs. Resistivity (p-type)

History

#	Item	Name / Type	Effective Date	Contents, Notes
1	Establish-ment	JSNM-SI-003 Test Method	20230314	Initial release (Japanese version)
Initi	Revision	JSNM-SI-003A Test Method	20240909	Initial release (English version)

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